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Enhanced photosensitive of Schottky diodes using SrO interfaced layer in MIS structure for optoelectronic applications

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ABSTRACT

In this study, the Schottky diodes (SDs) based on an interfacial layer of strontium oxide (SrO) thin film were fabricated. Thin films (TFs) were coated on glass and silicon substrates by low-cost spray pyrolysis coating technique with varying substrate temperatures of 350, 400, 450, and 500°C. Structural, surface morphology, optical, and electrical characteristics of SrO TFs were investigated. In particular, the I–V characteristics of Cu/SrO/n-Si diodes in dark and light excitations were analyzed. The maximum barrier height (Φ_B) for the diode fabricated at 500°C under Xenon lamp light irradiation was observed at 0.82 eV. Also, near ideal ideality factor (n) of the diode parameters, it was found at highest substrate temperature at 500°C. The results show that diodes are more fitting for the improvement of good quality photodiodes as well photodetector applications.

1. Introduction

In the modern era, electronic devices based on silicon (Si), germanium (Ge), and gallium (Ga) wafer substrates are widely performed. Among them, Si wafers are popularly used due to their low cost, abundance in Earth's crust, magnificent mechanical properties, and higher melting point compared with other semiconductor materials. Si has less reverse bias current, so power consumption is relatively low. However, compared with Ge and Ga, Si exhibits higher resistance and higher threshold voltage due to the low free electron concentration [1–5].

There has been progressing in thin film synthesis technology using physical, chemical, and solution deposition methods [6–19]. The Jet Nebulizer Spray Pyrolysis techniques (JNSP) have attracted the attention of researchers due to their low maintenance and simple handing and effectiveness for large scale high-quality films with acceptable prices, compared with other deposition methods. For instance, Marnadu et al. [19,20] successfully fabricated high quality thin films such as WO₃.

 $MoO_3,$ and $V_2O_5.$ Perumal et al. [21] Sr included HfO_2 thin films prepared by JSNP technique.

Recently, metal-insulator-semiconductor (MIS)-based SDs emerge as a representative device in electronic applications because of its extraordinary interfacial layer between metal and semiconductor. Various oxide materials such as MoO₃, HfO₂, WO₃, V₂O₅, and SrO are utilized as interfacial layers on the SD performance [22–25]. Among them, SrO TFs have attracted interest as optoelectronic devices since it exhibits high dielectric constant, low conductive losses, high permeability, excellent chemical thermal stability, and good insulating properties. However, reports on SrO interfacial layers in MIS-based SD applications are not adequately explored and understood.

Here, we demonstrate a new Schottky diode using SrO films which are prepared by JSNP technique and the influence of substrate temperature on structural, morphology, and the optical property. Additionally, Cu/SrO/n-Si diodes were fabricated, and their I–V and J-V characteristics parameters are investigated and analized in depth. As a

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V. Balasubramani et al.

Table 1

Parameter with their values.

Parameters	Values
Diameter of the nozzle	0.5 mm
Distance between substrate and nozzle	5 cm
Pressure maintained	3.5 kg cm ⁻²
Flow rate	0.5 ml min^{-1}
Time of spray	15 min
Substrates temperature	350°C, 400°C, 450°C and 500°C



Fig. 1. X-ray diffraction pattern of SrO films.

result, the performance of SrO-based photodiodes is significantly enhanced at optimized experimental conditions.

2. Experiment and characterization

2.1. Thin film and Schottky barrier diode preparation

Strontium Chloride (SrCl₂, 99.99%, Sigma-Aldrich) and Si substrate $(1 \times 1 \text{ cm}^2)$ were collected for preparing the pure SrO TFs. SrCl₂ was dissolved using ethanol individually and stirred for half an hour. The organized solution of 10 ml was sprayed on well-cleaned glass substrate

via JNSP method. The temperature of the substrate remains varying temperature from 350° C to 500° C. Deposition conditions for JNSP technique are tabulated in Table 1.

2.2. Characterization methods

The structure and surface morphology of SrO TFs has been performed via XRD (Rigaku Miniflex-II, CuK α , $\lambda = 1.5418$ Å) in range of 10–70° and atomic force microscope (AFM, model: 5100 Pico LE). Further investigations of the optical properties of TFs were performed using a UV–Vis spectrophotometer (JASCO, model: V–770 PC) in the wavelength range of 300–800 nm. DC electrical conductivity of the SrO TFs and I–V characteristics of Cu/SrO/n-Si type Schottky barrier diodes and switch response were investigated by Keithley's electrometer model No 6517-B.

3. Results and discussions

3.1. X-ray diffraction (XRD) investigation

Fig. 1 reveals the XRD patterns of the SrO TFs coated at different substrate temperatures at 350, 400, 450, and 500° C. All specimens show diffraction peaks at 22.58, 31.93, and 45.51° which correspond to the (220), (400), and (204) of SrO TFs (JCPDS No 01–0886), respectively. When the specimens were prepared at higher substrate temperatures, other peaks appear at 13.10, 39.41, 38.69, 40.58, and 62.24° corresponding to 111, 311, 420, 422, 116, 224, and 220 planes, respectively. Crystalline parameters such as FWHM, micro strain, dislocation density, and stacking fault were calculated using equations (1)–(4).

$$D = \frac{k\lambda}{\beta\cos\theta} \tag{1}$$

$$\boldsymbol{\varepsilon} = \boldsymbol{\beta} \frac{\cos \boldsymbol{\theta}}{4} \tag{2}$$

$$\delta = \frac{1}{D^2} \tag{3}$$

$$SF = \left[\frac{2\pi^2}{45(3\tan\theta)^{\frac{1}{2}}}\right]\beta$$
(4)

where, k-is constant value (0.9), λ -is incident beam wavelength, β -is FWHM of peak, and θ -is an angle of XRD diffraction position.

The calculated values of the crystalline parameters of TFs are listed in Table 2. It is observed that the average crystalline size (D) of TFs was found to be decreasing of 84.44, 80.75, 75.24, and 72.73 nm as increasing substrate temperature by 350, 400, 450, and 500°C, respectively. At higher temperatures, the removal of imperfections in the lattice and dislocation density in the TFs become larger leading to reduce crystalline. The reduction of grain size due to enhanced quality crystalline maybe decrease the grain boundary fraction and electrical resistivity of TF_S [26,27]. Moreover, the dislocation density value and micro strain show in the range from 1.0812 to 6.5946×10^{14} lines/m² and 0.00018 to 0.0041, respectively, which indicate the proving crystallinity at a higher substrate temperature of 500°C.

Table 2

Structural parameters of the SrO thin films.

Substrate temp (°C)	Diffraction 2(θ) (°)	Inter Planar Distance (d) (Å)	FWHM (Radians)	Crystallite Size(D)nm	Dislocation Density (δ) (10 ¹⁴ lines m ⁻²)	Micro Strain (ϵ)
350	31.89	2.8035	0.0170	84.44	1.4023	0.0041
400	13.20	6.7073	0.00145	95.73	1.0910	0.0036
	22.67	3.9223	0.00350	40.40	6.1263	0.00085
	25.95	3.4335	0.00233	60.97	2.6894	0.00056
	31.99	2.7969	0.0087	16.47	3.6838	0.0021
	39.54	2.2790	0.00350	42.09	5.6433	0.000824
450	13.10	6.7583	0.00145	95.72	1.0912	0.000362
	22.58	3.9374	0.00233	60.59	2.7236	0.000572
	31.93	2.8021	0.00116	12.36	6.5446	0.000280
	39.41	2.2859	0.00700	21.03	2.2602	0.001649
500	13.15	6.6583	0.0015	95.92	1.0812	0.000462
	22.64	3.7374	0.0026	60.19	2.7936	0.000372
	31.80	2.8021	0.0017	12.76	6.5946	0.000180
	39.39	2.1859	0.0072	21.83	2.2102	0.001749
	38.69	2.3268	0.0011	12.59	6.3033	0.000275
	40.58	2.2265	0.0010	13.85	5.2127	0.000250
	45.51	1.9913	0.0056	26.41	1.4332	0.001313
	62.24	1.4902	0.0017	91.05	1.2062	0.000380



Fig. 2. Absorption (a) and Tauc's plot (b) of SrO films.

Table 3Band gap energy value SrO thin films.

Sample Code	Band gap (Eg) (eV)
350°C	3.91
400°C	3.84
450°C	3.78
500°C	3.73

3.2. Optical property

Fig. 2(a) shows the absorbance and Tauc's plot spectroscopy in the range from 200 to 800 nm of SrO TFs with different substrate temperatures. The absorption shows the peak at around 340 nm with the intensity of absorptions slightly increasing with increasing ST owing to growing TFs thickness. TFs thickness is one of the important features of optical property. It not only affects the intensity absorption but also affects the cluster size and crystalline size of the film. This leads to the density of the free electrons and optical bandgap [28,29]. Fig. 2(b) exhibits the E_{opt} of films that are estimated by extrapolating direct transition (n = 2) using linear Tauc's plot as represented by the flowing relation.

$$\alpha \hbar \nu = B \left(\hbar \nu - E_g \right)^n \tag{5}$$

where, α is the absorption co-efficient, h is the Planck's constant, υ is the incident photon energy, B is the constant and E_g is the optical band energy of the films.

The calculated interrupts of the plots are established to optical band gap values 3.91, 3.84, 3.78, and 3.73 eV consistent at 350, 400, 450, and 500°C, respectively (Table 3). The decrease of E_{opt} may be due to the effect of thickness on crystalline size and defects of TFs [30–32]. Notably, film coated at 500°C film displays the highest absorbance and minimum bandgap caused by the high crystalline size and plane surface compared with other concentrations it is evinced by XRD. Additionally, TFs having high absorbance is appropriate for engineering applications, particularly optoelectronic applications.

3.3. AFM analysis

Fig. 3 displays 2-D and 3-D images from the AFM technique with (5 μ m×5 μ m) resolution of SrO TFs. Surface grains are fairly smooth surface hillock structures due to the surface effect and/or the surface impurities. Similarly, this one can be found that the surfaces are disposed to be receiving denser so as to make the spaces among grains get smaller



Fig. 3. AFM topography view of SrO films.

and even merge or vanish with thinner films, which is helpful in reducing leakage current density and dielectric loss [33,34]. AFM pictures confirm the development of an even layer of the SrO on n-Si surface which would be good for the diode fabrication.

3.4. Electrical Property

3.4.1. DC electrical conductivity

The electrical conductivity (odc) observed by Keithley source upon from 10 to 100 V voltage constants with varying temperatures $30-120^{\circ}$ C, as shown in Fig. 4. I–V characteristics of the TFs with different substrate temperatures of 350, 400, 450, and 500°C are observed using the following equation. Table 4 shows the electrical conductivity and activation energy values. The conductivity films increase from 6.281×10^{-14} to 1.605×10^{-10} S/cm as increasing substrate temperatures.

$$\sigma_{dc} = (d / A).(I / V) S/cm$$
(6)

where I is the current, V is the applied voltage, d is the inter-probe distance and A is the cross-sectional area of the film. Arrhenius plot, Fig. 5, reveals the activation energy (E_a) of SrO films. The varying of E_a values from 0.0709 to 0.0239 eV with different substrate temperatures may be due to imperfection of a crystal lattice, surface roughness, and the bounding of electrons [35]. Notably, the film coated at 500°C displays the lowest amount of activation energy and upper conductivity values which match with the result from the crystalline, smooth surface, and optical property analyses.

3.4.2. Evaluation Cu/SrO/n-Si type Schottky barrier diode

Cu/SrO/n-Si with different substrate temperatures of 350, 400, 450, and 500°C are carried out forward and reverse bias to recognize the current transportation mechanism. Semilogarithmic I–V plot, Fig. 6, shows a linear behavior at the moderate voltage and then deviated from the linearity at enough high forward bias voltages due to the effect of the series-resistance, interfacial layer, and surface states (N_{ss}). The semiconductor device/structures with R_s , Nss, and an interfacial layer were applied bias voltage (Vi) crossways that will be jointed via interfacial layer and surface states as: Va = Vi + VRs + VD + Vit. This leads to the I–V plot diverging from the linearity at sufficient high forward bias voltages. On the other hand, while the value of Rs and interfacial layer are in effect at high bias voltages, N_{ss} is effective for intermediate bias voltage. The behavior of diodes was affected by parameters of films such as growth temperature, atomic sizes, MIS interface layer, trap interface, and the formation of barrier height from the thermionic emission theory [36–41]. The current through a Cu/SrO/n-Si of SD at forwarding bias can be written as below equations [42].

$$I = AA^*T^2 exp(-q\Phi_B/kT).[exp(qV/nkT)-1)]$$
(7)

$$I_0 = AA^*T^2 \exp\left(-q\Phi_B/kT\right) \tag{8}$$

where I_0 is the reverse saturation current, q is the electron charge, V is the applied voltage, n is the ideality factor, k is the Boltzmann constant, and T is the absolute temperature. The I_0 values were observed using concluding from the zero practical voltage cut via the linear in-between voltage area, as listed in Table 5. Fig. 7(a and b) shows the schematic diagram SD and the energy level band diagram of the Cu/SrO/n-Si MIS SD device. At room temperature without upon voltage, the Fermi level in MIS structure is usually pinioned due to the contact effect between the interface of metal and semiconductor [43]. Carriers from metal can inject to semiconductor and form the barrier height (Φ_B) with ideality factor (n) as the following equation:

$$n = \frac{q}{K_B T} \frac{dV}{d(\ln I)} \tag{9}$$

$$\boldsymbol{\phi}_{\mathrm{B}} = \mathrm{k.T/q} \ln \left(AA^* T^2 / \mathrm{I_0} \right) \tag{10}$$

The calculated ideality factor values have not equal to one and if n equals one, pure thermionic emission occurs but then n is commonly



Fig. 4. Current Vs Voltage plot of SrO films.

Table 4Electrical parameters for SrO thin films.

Sample Code	Conductivity (S/cm)	Activation energy (eV)
350°C 400°C 450°C 500°C	$\begin{array}{c} 6.281\times 10^{-14}\\ 1.432\times 10^{-12}\\ 2.352\times 10^{-12}\\ 1.605\times 10^{-10}\end{array}$	0.0709 0.0704 0.0241 0.0239

larger than unity. The value of n (=1+ di/ ϵ_i (ϵ_s/W_d + qN_{ss})) is dependent on a lot of parameters such as the existing native or deposited interfacial layer, both its thickness (d_i) and permittivity (ϵ_i), barrier inhomogeneity at the junction with numerous lower barriers/patches or pinch off at round mean BH, Depletion layer width (W_d= ($2\epsilon_s.\epsilon_oV_d/qN_d$)^{0.5}) or the level of doping donor atoms, surface states (N_{ss}) [44,45].

Carriers freely permit through lower barriers or patches leading to an increase in the current or ideality factor. The formation surface states in the bandgap of semiconductors can capture and release some electrons under electric field and phonon due to recombination centers. Table 5 demonstrates the Zero-bias BH (Φ_{Bo}) values increase while the values of n decrease with increasing substrates temperature in both dark and light excitation cases. The nature and origin of the change of Φ_{Bo} and n have



Fig. 5. Arrhenius plot of SrO films.



Fig. 6. Forward and reverse-bias ln (J)-V characteristics of the Cu/SrO/n-Si Schottky diode.

Table 5
Schottky diode parameters like n, Φ_B , and I_0 , are tabulated.

Light	Dark	Light	Dark (10 ⁻⁶)	Light(10 ⁻⁴)
0.72 0.75 0.79	3.57 2.97 2.30	3.35 2.75 2.13	9.73 6.79 4.89	7.85 5.98 3.75
	0.72 0.75 0.79 0.82	Dark Dark 0.72 3.57 0.75 2.97 0.79 2.30 0.82 1.89	O.72 3.57 3.35 0.75 2.97 2.75 0.79 2.30 2.13 0.82 1.89 1.73	O.72 3.57 3.35 9.73 0.75 2.97 2.75 6.79 0.79 2.30 2.13 4.89 0.82 1.89 1.73 2.76

been clarified by thermionic theory with a Gaussian distribution (GD) of the barrier heights [46–49].

At low temperatures, charge carriers can transport from lower barriers or patches located around the mean barrier height, leading to an increase in the barrier height which is called apartment BH. At higher temperatures, these charges are balanced by the considerable in the uniform region, therefore, almost currents flow via the uniform region or high BH. This leads to the increase of BH rises and the decrease of ideality factor with increasing temperature. In this case, the relation between BH and ideality factor is presented: Φ_B (T) = Φ_{Bo} (T)-(tan0.n.), here Φ_{Bo} is the mean BH for n = 1. Thus, the mean value of BH was



Fig. 7. (a) Schematic diagram and (b) energy level band diagram of Cu/SrO/n-Si Schottky diode.

observed as 0.873 eV for n = 1. For n > 1, the diode was impacted by its characterizations such as interface states, non-consistency dispersion of the interfacial charges, recombination-age, series obstruction, burrowing impact, picture force impact, extra capacitance, voltage drop present at the interfacial layer, and conceivable outcomes, leading to inhomogeneity boundary tallness [50].

4. Conclusion

Colossal photosensitive lift in Cu/SrO/n-Si SD has been successfully fabricated by JNSP technique. The influence of substrate temperature on structural parameters, optical properties, and surface roughness of SrO film was investigated. AFM pictures confirmed the fairly smooth surface hillock structure and development of an unbroken layer of the SrO on n-Si surface. The I–V characteristic diode parameters of Cu/SrO/n-Si diodes gigantic photosensitive lift in under light irradiation. The maximum barrier height (Φ_B) for the diode fabricated at 500°C in under light irradiation was observed at 0.82 eV. Also, near ideal ideality factor (n) of the diode parameters, it was found for film coated at 500°C ST. Overall that fabricated diodes are more fitting for the improvement of high-quality photodiodes and optoelectronic applications.

CRediT authorship contribution statement

V. Balasubramani: processed the samples, compiled and analyzed the data, Writing – original draft, Supervision. Phuong V. Pham: Writing – review & editing. A. Ibrahim: Validation, Writing – review & editing. Jabir Hakami: Writing – review & editing. Mohd Zahid Ansari: Writing – review & editing, Supervision. Top Khac Le: Supervision, Writing – review & editing, All authors have read the final manuscript and confirmed its content.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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V. Balasubramani et al.

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